**256× 4b的RAM模块：**

module RAM\_256(A,Din,Dout,clk,str,sel,ld,clr);

input [7:0] A;//地址

input [3:0] Din;

input clk,str,sel,ld,clr;

output reg[3:0] Dout;

integer i;

reg [3:0] data[255:0]; //memory型，256个存储单元的存储器data，每个存储单元是一个4 //位寄存器

initial begin

Dout = 4'bz;

end

always@(posedge clk or posedge clr)

begin

if(sel == 0) begin Dout = 4'bxxxx; end

else

begin

if(clr == 1)

begin

for(i = 0; i < 255; i = i+1)

data[i] = 0;

end

else if(str == 1)

begin

data[A] = Din;

end

else if(ld == 1)

begin

Dout = data[A];

end

else begin Dout = 4'bz; end

end

end

endmodule

**2\_4译码器：**

module yima2\_4(in,out);

input [1:0]in;

output reg[3:0] out = 1;

always@(in)

begin

case(in)

2'b00: out = 4'b0001;

2'b01: out = 4'b0010;

2'b10: out = 4'b0100;

2'b11: out = 4'b1000;

endcase

end

Endmodule

**顶层文件，1K× 8b的RAM：**

module RAM\_1k(A,Din,Dout,clk,str,ld,sel,clr,out);

input [9:0] A;

input [7:0] Din;

input clk,str,ld,sel,clr;

output [7:0]Dout;

output [3:0]out;

yima2\_4 yima1(.in(A[9:8]),.out(out));

RAM\_256 RAM0(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0001)),.ld(ld &(out == 4'b0001)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM1(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0001)),.ld(ld &(out == 4'b0001)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM2(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0010)),.ld(ld &(out == 4'b0010)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM3(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0010)),.ld(ld &(out == 4'b0010)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM4(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0100)),.ld(ld &(out == 4'b0100)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM5(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0100)),.ld(ld &(out == 4'b0100)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM6(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b1000)),.ld(ld &(out == 4'b1000)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM7(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b1000)),.ld(ld &(out == 4'b1000)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

endmodule

**1K× 8b的RAM测试文件：**

module RAM\_1k(A,Din,Dout,clk,str,ld,sel,clr,out);

input [9:0] A;

input [7:0] Din;

input clk,str,ld,sel,clr;

output [7:0]Dout;

output [3:0]out;

yima2\_4 yima1(.in(A[9:8]),.out(out));

RAM\_256 RAM0(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0001)),.ld(ld &(out == 4'b0001)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM1(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0001)),.ld(ld &(out == 4'b0001)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM2(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0010)),.ld(ld &(out == 4'b0010)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM3(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0010)),.ld(ld &(out == 4'b0010)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM4(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b0100)),.ld(ld &(out == 4'b0100)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM5(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b0100)),.ld(ld &(out == 4'b0100)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

RAM\_256 RAM6(.A(A[7:0]),.Din(Din[7:4]),.clk(clk),.str(str &(out == 4'b1000)),.ld(ld &(out == 4'b1000)),.sel(sel),.clr(clr),.Dout(Dout[7:4]));

RAM\_256 RAM7(.A(A[7:0]),.Din(Din[3:0]),.clk(clk),.str(str &(out == 4'b1000)),.ld(ld &(out == 4'b1000)),.sel(sel),.clr(clr),.Dout(Dout[3:0]));

Endmodule

**256× 4b的RAM测试文件：**

module RAM\_256(A,Din,Dout,clk,str,sel,ld,clr);

input [7:0] A;//??

input [3:0] Din;

input clk,str,sel,ld,clr;

output reg[3:0] Dout;

integer i;

reg [3:0] data[255:0]; //?256?????????????4????

initial begin

Dout = 4'bz;

end

always@(posedge clk or posedge clr)

begin

if(sel == 0) begin Dout = 4'bxxxx; end

else

begin

if(clr == 1)

begin

for(i = 0; i < 255; i = i+1)

data[i] = 0;

end

else if(str == 1)

begin

data[A] = Din;

end

else if(ld == 1)

begin

Dout = data[A];

end

else begin Dout = 4'bz; end

end

end

endmodule